Confirmation No. 3872

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	GOFF	Examiner:	Mamo, E.
Serial No.:	10/538,458	Group Art Unit:	2184
Filed:	June 10, 2005	Docket No.:	US020598US2
Title:	ENCAPSULATED HARDWARE CONFIGURATION/CONTROL		

APPEAL BRIEF

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P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed July 23, 2008 and in response to the rejections of claims 1-13 as set forth in the Final Office Action dated March 26, 2008 and in further response to the Advisory Action dated June 6, 2008.

Please charge Deposit Account number 50-0996 (NXPS.353PA) $510.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017413/0445 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-13 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action dated March 26, 2008.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a method of performing configuration or control of a subsystem (*see, e.g.*, hardware subsystem 110 shown in Fig. 1, and page 2:23-26). The method includes providing together with the subsystem a configuration/control unit having a controller portion (*see, e.g.*, configuration/control state machine 113 shown in Fig. 1, and page 2:27-30) and a storage portion (*see, e.g.*, read only memory 115 shown in Fig. 1, and page 2:27-30) storing configuration parameters; the configuration/control unit receiving an activation signal (*see, e.g.*, page 3:1-3); and the configuration/control unit, in response to the activation signal, performing configuration or control of the subsystem, including storing at least one of the configuration parameters in a register of the subsystem (*see, e.g.*, registers 111 shown in Fig. 1, page 2:27-30, and page 3:1-7).

Commensurate with independent claim 6, an example embodiment of the present invention is directed to a subsystem having self-configuration capabilities (*see, e.g.*,

hardware subsystem 110 shown in Fig. 1, and page 2:23-26). The subsystem includes a register section including multiple registers (*see, e.g.*, registers 111 shown in Fig. 1, and page 2:27-30), the subsystem functioning differently depending on contents of the registers; and a configuration/control unit having a controller portion (*see, e.g.*, configuration/control state machine 113 shown in Fig. 1, and page 2:27-30) and a storage portion (*see, e.g.*, read only memory 115 shown in Fig. 1, and page 2:23-26) storing configuration parameters; wherein the configuration/control unit is responsive to an activation signal for performing configuration or control of the subsystem, including storing at least one of the configuration parameters in one of the multiple resisters of the subsystem (*see, e.g.,* page 3:1-7).

Commensurate with independent claim 11, an example embodiment of the present invention is directed to, for use in a system that includes a processor (*see, e.g.*, processor 101 shown in Fig. 1, and page 2:16-22) coupled to a hardware subsystem (*see, e.g.*, hardware subsystem 110 shown in Fig. 1, and page 2:23-26) via a system bus (*see, e.g.*, system bus 103 shown in Fig. 1, and page 2:16-22), the hardware subsystem including a configuration/control unit (*see, e.g.*, configuration/control state machine 113 and read only memory 115 shown in Fig. 1, and page 2:27-30) and a plurality of registers (*see, e.g.*, registers 111 shown in Fig. 1, and page 2:27-30), a method of configuring the subsystem. The method includes storing a plurality of configuration parameters in the configuration/control unit (*see, e.g.,* page 3:8-11); and responsive to the configuration/control unit receiving a single configuration/control ID from the processor, writing one or more of the plurality of configuration parameters from the configuration/control unit to one or more of the plurality of registers (*see, e.g.,* page 3:1-7).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject

matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

A. Claims 1-12 stand rejected under 35 U.S.C. § 103(a) over Martel *et al.* (U.S. Patent No. 5,887,165).

B. Claim 13 stands rejected under 35 U.S.C. § 103(a) over Martel in view of Wu *et al.* (U.S. Patent No. 6,862,643).

VII. Argument

A. The rejection of claims 1-12 under U.S.C. § 103(a) over Martel should be reversed because Martel fails to disclose each recited claim limitation and because no valid reason has been presented to modify Martel.

The § 103 rejection must be reversed because each and every recited claim element is not taught by the cited references. As discussed under Section 3, *supra*, the Examiner acknowledges that the Martel reference does not teach storing a plurality of configuration parameters, but, rather, relies on Official Notice that one could and would modify Martel to do as such. Applicant challenged these assertions but the Examiner refused to respond consistent with M.P.E.P. § 2144.03. Moreover, the Martel reference fails to teach a configuration/control unit that receives an activation signal and Martel fails to teach a hardware subsystem that receives a configuration/control ID from a processor that is external to the subsystem.

The claimed invention is directed to an important advancement involving an encapsulated reconfigurable hardware subsystem that is responsive to a configuration/control ID, which is provided to the subsystem from an external processor. Appellant's reconfigurable hardware subsystem is configured by writing configuration parameters stored in the subsystem's configuration/control unit to registers of the subsystem responsive to the configuration/control ID. The configuration of the subsystem depends on which of the configuration parameters are written in the registers. Thus, different configuration/control IDs can be used to implement different

configurations of the hardware subsystem. Appellant's invention enables a system programmer to configure the subsystem using configuration/control IDs without needing to be concerned with details of the functionality of the subsystem. A detailed discussion of the specific differences between the subject matter of the claims and the asserted Martel reference is provided below.

1. The rejection of claims 1-10 under U.S.C. § 103(a) over Martel should be reversed because Martel fails to disclose a configuration/control unit receiving an activation signal and, in response thereto, configuring a subsystem.

The § 103(a) rejection of claims 1-10 must be reversed because Martel fails to teach or suggest aspects of the claimed invention directed to a configuration/control unit, which includes a controller, receiving an activation signal and, in response thereto, configuring the subsystem. The Examiner's assertion that Martel's CPU 17 receives a configuration signal is directly contradicted by Martel who teaches that CPU 17 (*i.e.,* the Examiner's alleged controller) provides a configuration signal (*i.e.,* the Examiner's alleged activation signal) to configuration memory 19 and gate array 13. *See, e.g.,* Figure 1. Appellant notes that the Examiner acknowledges that Martel discloses that the processor/controller 17 sends the configuration signal. *See, e.g.,* page 2:4-5 of the Advisory Action dated 6/6/2008. Martel's CPU 17 provides the configuration signal, instead of receiving the configuration signal and configuring the subsystem in response to the configuration signal as does Appellant's configuration/control unit. Thus, Martel's CPU 17 does not correspond to Appellant's controller portion of the configuration/control unit.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 1-10 fails, and therefore must be reversed.

2. The rejection of claims 11-12 under U.S.C. § 103(a) over Martel should be reversed because Martel fails to disclose a configuration/control unit receiving a configuration/control ID from a processor.

The § 103(a) rejection of claims 11-12 must be reversed because Martel fails to teach or suggest aspects of the claimed invention directed to a configuration/control unit

receiving a single configuration/control ID from the processor, and responsive thereto, writing one or more of the configuration parameters, which are stored in the configuration/control unit, to one or more of a plurality of registers. The Examiner erroneously asserts that Martel's configuration memory 19 corresponds to Appellant's configuration/control unit and that Martel's controller (*i.e.,* CPU 17) corresponds to Appellant's processor. *See, e.g.,* Figure 1. Appellant submits that it would be readily apparent to the skilled artisan that Martel's configuration memory 19 does not correspond to the claimed configuration/control unit which can be, for example, a state machine (*see, e.g.,* claim 12). *See, e.g.,* M.P.E.P. § 2111 ("The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach.").

Moreover, Appellant's processor is coupled to a hardware subsystem (which contains the configuration/control unit) via a system bus (*i.e.,* Appellant's processor is not part of Appellant's hardware subsystem). The Examiner, however, alleges that Martel's reconfigurable hardware system 11 corresponds to Appellant's hardware subsystem (*see, e.g.,* page 5 of the Final Office Action dated 3/26/2008) and Martel teaches that CPU 17 (*i.e.,* the Examiner's alleged processor) is part of the reconfigurable hardware system 11. *See, e.g.,* Figure 1 and Col. 3:38-43. Thus, Martel's CPU 17 does not correspond to Appellant's processor.

Regarding claim 12, Appellant notes that the Examiner discusses Martel's controller (*i.e.,* CPU 17), which has been asserted by the Examiner as corresponding to Appellant's processor, not Appellant's configuration/control unit. Moreover, the cited portions of Martel do not teach that CPU 17 can be a state machine. *See, e.g.,* Figure 1 and Col. 2:49.

The Examiner, in the Advisory Action dated 6/6/2008, now appears to be asserting that Martel's gate array 13 corresponds to Appellant's configuration/control unit. *See, e.g.,* page 2:6-9 of the Advisory Action. The Examiner, however, appears to also be asserting that Martel's gate array 13 (*i.e.,* reconfigurable logic module) corresponds to Appellant's plurality of registers. *See, e.g.,* page 5 of the Final Office Action. Appellant submits that the Examiner's apparent shifting interpretation regarding the alleged correspondence between the cited portions of Martel and the claimed invention is due to the fact that Martel does not teach or suggest a processor (which is not

part of a hardware subsystem) that sends a configuration/control ID to a configuration/control unit (which is part of the hardware subsystem).

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 11-12 fails, and therefore must be reversed.

3. The rejection of claims 1-12 under U.S.C. § 103(a) over Martel should be reversed because the Examiner improperly relies upon Official Notice and because no valid reason has been presented to modify Martel.

The § 103(a) rejection of claims 1-12 must be reversed because the Examiner improperly relies upon Official Notice without accompanying documentary support, because the Examiner refused to respond consistent with M.P.E.P. § 2144.03 to Appellant's request for such documentary support, and because no valid reason to modify the Martel reference has been presented.

The Examiner's reliance upon Official Notice is based on the undisputed fact that Martel does not teach storing more than one configuration parameter in configuration memory 19. *See, e.g.,* page 3:3-4 of the Final Office Action dated 3/26/2008. This aspect is important to the claimed invention "as a whole" because storing a plurality of configuration parameters allows the subsystem to be configured in different manners responsive to the receipt of different configuration/control IDs (*i.e.,* the subsystem can be reconfigured by providing only a single configuration/control ID). Ignoring this relationship, the Examiner then asserts that "it would have been an obvious matter of alternate arrangement to store more than one/multiple/many/plurality of configuration parameters".

In terms of correspondence, the Examiner has not cited to any reference that teaches storing a plurality of configuration parameters and the Examiner has not cited to any reference to support the conclusion that it would be obvious to store a plurality of configuration parameters. Appellant challenged the Examiner's use of Official Notice (*see, e.g.,* page 6 of the Response dated 5/27/08) to which the Examiner refused to respond consistent with M.P.E.P. § 2144.03 ("It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being

well-known"). Appellant submits that it is not capable of instant and unquestionable demonstration that storing a plurality of configuration parameters is well-known, which is why Appellant previously requested that the Examiner provide documentary evidence to support such a conclusion. *See, e.g.,* M.P.E.P. § 2142 ("rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness").

The Examiner responded to Appellant's request, not by providing documentary evidence, but instead by citing authority that is inapplicable to the Examiner's unsupported conclusion. *See, e.g.,* page 2:10-13 of the Advisory Action dated 6/6/2008 citing *In re Rose* 105 USPQ 237 (CCPA 1955). The holding *In re Rose* concerns limitations relating to the physical size of a package, which were not deemed sufficient to patentably distinguish over the prior art. *See, e.g.,* M.P.E.P. § 2144.04(IV)(A). In contrast, Appellant's claims do not recite any limitations relating to size or dimensions. As such, Appellant submits that the Examiner's reliance upon *In re Rose* is unfounded. Thus, the rejections are improperly based upon mere unsubstantiated conclusory statements and the Examiner's reliance upon Official Notice unaccompanied by documentary support is improper.

In terms of motivation, the Examiner fails to provide a valid reason why the skilled artisan would modify the Martel reference to store a plurality of configuration parameters. The mere fact that the skilled artisan could rearrange the parts of the reference device to meet the terms of the claims is not by itself sufficient to support a finding of obviousness. The Examiner must also provide a motivation or reason for the skilled artisan, without the benefit of Appellant's specification, to make the necessary changes in the reference device. *See, e.g.,* M.P.E.P. § 2144.04. The Examiner, in the Final Office Action dated 3/26/2008, failed to provide any reason why the skilled artisan would modify the Martel reference. The Examiner tacitly acknowledged the failure of the Final Office Action to provide any reason to modify Martel by attempting to provide such a reason in the Advisory Action dated 6/6/2008 (*see* page 3:16-18). This rational, raised for the first time in the Advisory Action, is not at issue in this Appeal. Rather, the Examiner has raised new grounds of rejection in a failed effort to maintain the averment of obviousness. Should the Board consider these new grounds, Appellant submits that

the Examiner once again fails to provide a valid reason why the skilled artisan would modify the Martel reference.

Specifically, in the Advisory Action, the Examiner asserts that the skilled artisan would modify Martel to store a plurality of configuration parameters so that "the hardware system can be configured for different applications that require different data transfer protocols or operation modes." *See, e.g.,* page 2:16-18. The Martel reference, however, already allows the field programmable gate array 13 to be configured for different applications, for example, configuration data can be retrieved not just from configuration memory 19, but also from remote computers 33 and 35. *See, e.g.,* Figure 1 and Col. 5:20-25. Thus, the Examiner's alleged reason to modify Martel is to address a problem already solved by Martel. The requirement that the motivation for the combination be articulated has been clearly set forth in *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). Moreover, 35 U.S.C. 103(a) requires that the rejection of a claim be addressed under the "as a whole" inquiry. When the asserted reason for the skilled artisan to combine the prior-art teachings is based on an alleged problem, the inquiry requires consideration of whether the alleged problem is an actual problem as properly articulated in the Office Action or, rather, the problem has been concocted in an effort to employ improper hindsight. See, e.g., USPTO Guidelines for § 103 rejections after *KSR,* and M.P.E.P. § 2141.02. Thus, it is improper to combine references without any real motivation, such as here, where a nonexistent problem is being addressed by the Examiner.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 1-12 fails, and therefore must be reversed.

4. The rejection of claims 4 and 10 under U.S.C. § 103(a) over Martel should be reversed because Martel fails to disclose a configuration/control unit that is responsive to multiple different configuration/control IDs.

The § 103(a) rejection of claims 4 and 10 must be reversed because Martel does not teach or suggest multiple different configuration/control IDs, responsive to which, the configuration/control unit performs different corresponding configurations of the

subsystem. Specifically, Martel only teaches a single activation signal that causes the hardware configuration stored in configuration memory 19 to be established in the reconfigurable logic module 13. *See, e.g.,* Figure 1 and Col. 2:7-16. Martel does not mention multiple different activation signals or that multiple hardware configurations are stored in the configuration memory 19. Martel simply establishes the hardware configuration stored in configuration memory 19 in the reconfigurable logic module 13 in response to the activation signal.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claims 4 and 10 fails, and therefore must be reversed.

B. The rejection of claim 13 under U.S.C. § 103(a) over Martel in view of Wu should be reversed because the cited combination does not correspond to the claimed invention and because no valid reason has been presented to modify Martel.

The § 103(a) rejection of claim 13, which depends from claim 11, must be reversed for at least the same reasons discussed above in regard to claim 11 in Sections 2 and 3. As a first example, Martel does not teach a configuration /control unit, which is part of a subsystem, that receives a configuration/control ID from a processor that is external to the subsystem and Martel does not teach storing a plurality of configuration parameters in the configuration /control unit. Appellant submits that the addition of the Wu reference provides nothing that would overcome these deficiencies. As a second example, due to the Examiner's improper use of Official Notice in attempting to support modification of Martel to store a plurality of configuration parameters as discussed above in Section 3, any further modification of Martel based on Wu is also improper.

For at least the reasons presented above, Appellant submits that the § 103(a) rejection of claim 13 fails, and therefore must be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-13 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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Respectfully Submitted,

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/538,458)

1. A method of performing configuration or control of a subsystem, comprising: providing together with the subsystem a configuration/control unit having a controller portion and a storage portion storing configuration parameters; the configuration/control unit receiving an activation signal; and the configuration/control unit, in response to the activation signal, performing configuration or control of the subsystem, including storing at least one of the configuration parameters in a register of the subsystem.

2. The method of claim 1 wherein the subsystem is a hardware subsystem, and the configuration/control unit is a hardware configuration/control unit.

3. The method of claim 1 wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit.

4. The method of claim 1 wherein the activation signal is a configuration/control ID.

5. The method of claim 4 wherein the configuration/control unit is responsive to multiple different configuration/control IDs for performing different corresponding configuration or control actions with respect to the subsystem.

6. A subsystem having self-configuration capabilities, comprising: a register section including multiple registers, the subsystem functioning differently depending on contents of the registers; and a configuration/control unit having a controller portion and a storage portion storing configuration parameters; wherein the configuration/control unit is responsive to an activation signal for performing configuration or control of the subsystem, including storing at least one of the configuration parameters in one of the multiple resisters of the subsystem.

7. The apparatus of claim 6 wherein subsystem is a hardware subsystem, and the configuration/control unit is a hardware configuration/control unit.

8. The apparatus of claim 7 wherein the hardware subsystem and the hardware configuration/control unit are provided together within the same integrated circuit.

9. The apparatus of claim 6 wherein the activation signal is a configuration/control ID.

10. The apparatus of claim 9 wherein the configuration/control unit is responsive to multiple different configuration/control IDs for performing different corresponding configuration or control actions with respect to the subsystem.

11. For use in a system that includes a processor coupled to a hardware subsystem via a system bus, the hardware subsystem including a configuration/control unit and a plurality of registers, a method of configuring the subsystem comprising:

storing a plurality of configuration parameters in the configuration/control unit; and

responsive to the configuration/control unit receiving a single configuration/control ID from the processor, writing one or more of the plurality of configuration parameters from the configuration/control unit to one or more of the plurality of registers.

12. The method of claim 11, wherein the configuration/control unit is a state machine.

13. The method of claim 11, wherein the subsystem is a USB block comprising a plurality of ports that can operate in different modes responsive to which of the plurality of configuration parameters are written to which of the plurality of registers.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.